a second gate insulating film interposed therebetween, said second semiconductor layer comprising a second channel formation region and second source and drain regions being in contact with said second channel formation region,

wherein said second gate electrode partially overlaps said second source and drain regions, and

wherein a wiring is connected to said at least one of said second source and drain regions.

Cancel Claim 26.

REMARKS

Applicants will address each of the Examiner's objections and rejections in the order in which they appear in the Office Action.

I. Rejections Under 35 USC §112

In the Office Action, the Examiner has a number of specific objections to Claims 11-13 and 24-26 under 35 USC §112, second paragraph, for informalities in the claims. Applicants have amended Claims 11 and 24 and canceled Claims 13 and 26 to correct these informalities. It is respectfully submitted that as amended, the claims are in an allowable condition.

II. Prior Art Rejections

The Examiner also has a number of rejections under 35 USC §103. Applicants will address each in the order in which they appear in the Office Action.

A. Rejection Over Yamazaki et al.

The Examiner rejects Claims 1-4, 6-9, 14-17 and 19-22 under 35 USC §103 as being unpatentable over Yamazaki et al. This rejection is respectfully traversed.

Independent Claims 1, 6, 14 and 19 require that each gate electrode of said n-channel TFT and said p-channel TFT have a first conductive layer being in contact with a gate insulating film, and a second conductive layer being in contact with said gate insulating film and top and side surfaces of said first conductive layer.

The Examiner contends that Yamazaki discloses a first conductive layer of each gate electrode being the inner portion of each of gate electrodes 107, 113 being in contact with a gate insulating film 106, 112 and a second conductive layer being the outer portion of each of the gate electrodes 107, 113 being in contact with the gate insulating film and top and side surfaces of the first conductive layer. Applicants respectfully disagree with this interpretation of the reference as being improper.

As clearly shown in the figures in the present application, each of the gate electrodes of the claimed invention has a first and second conductive layer.

In contrast, there is no disclosure in Yamazaki of such first and second conductive layers. Instead, the Examiner has cited some alleged "inner portion" and "outer portion" of the gate electrodes in Yamazaki. However, Yamazaki contains no disclosure or suggestion of such inner or outer portion. There is nothing in the drawings or text showing such alleged portions.[1] Further, there is nothing in Yamazaki defining any ranges or dividing line between such alleged portions. Instead, Yamazaki shows a gate electrode with no distinct layers. Hence, Applicants believe that it is

[1] The undersigned did an electronic search in Yamazaki and could find no reference in the patent to an inner portion or outer portion of a gate electrode.

improper for the Examiner to allege that Yamazaki discloses the first and second conductive layers of the gate electrode, as recited in the claims.

Applicants respectfully submit that the basis for such alleged inner and outer portions in Yamazaki could only be arrived at by hindsight reconstruction using the claimed invention as a blueprint. Such a procedure is improper. See e.g. Ecolochem, Inc. v. Southern California Edison Company, 56 USPQ2d 1065, 1072-1076 (Fed. Cir. 2000). Hence, since the basis for this rejection is improper, it should be withdrawn.

Further, independent Claims 1, 6, 14 and 19 require a portion which said second conductive layer is in contact with said gate insulating film in said n-channel TFT partially overlaps said pair of LDD regions, and a portion which said second conductive layer is in contact with said gate insulating film in said p-channel TFT partially overlaps said second source and drain regions. Applicants respectfully submit that these features are not disclosed or suggested by Yamazaki.

Accordingly, for at least the above-stated reasons, the independent claims 1, 6, 14 and 19 and those claims dependent thereon are not disclosed or suggested by Yamazaki but are patentable thereover. Therefore, it is respectfully requested that this rejection be withdrawn.

B. Rejection Over Miyasaka et al.

The Examiner also rejects Claims 11-13 under 35 USC §103 as being unpatentable over Miyasaka et al. This rejection is also respectfully traversed.

Independent Claim 11 requires that the "second gate electrode partially overlaps the second source and drain regions." The Examiner alleges that Miyasaka shows a second gate electrode 6 which partially overlaps second source and drain regions 4, 10.

Applicants disagree with this interpretation of the reference. Region 10 in Miyasaka appears to be a LDD region, not a source or drain region, as required in the claim. Accordingly, Applicants respectfully submit that independent Claim 11 and those claims dependent thereon are not disclosed or suggested by the cited reference and are patentable thereover. Therefore, it is respectfully requested that this rejection be withdrawn.

C. Rejection Over Miyaska et al. in view of Johnson

The Examiner also rejects Claims 24-26 under 35 USC §103 as being unpatentable over Miyasaka et al. in view of Johnson. This rejection is also respectfully traversed.

Independent Claim 24 also requires that the "second gate electrode partially overlaps the second source and drain regions." As explained above, this feature is not disclosed or suggested by Miyasaka (and Johnson is not cited to show the feature).

Accordingly, Applicants respectfully submit that independent Claim 24 and these claims dependent thereon are not disclosed or suggested by the cited references and are patentable thereover. Therefore, it is respectfully requested that this rejection be withdrawn

Accordingly, for at least the above-stated reasons, it is respectfully submitted that the claims are patentable, and the rejections under §103 should be withdrawn.

Conclusion

It is respectfully submitted that the present application is now in a condition for allowance, and it is requested that it now be allowed.

If any fee is due for this amendment, please charge our deposition account 50/1039.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,

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